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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,692	07/28/2004	Sanish Koshi JACOB	TI-37611	4691

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EXAMINER	
JACKSON, STEPHEN W	
ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
11/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/710,692	JACOB, SANISH KOSHI	
	Examiner	Art Unit	
	Stephen W. Jackson	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *09 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 11-13* is/are pending in the application.

4a) Of the above claim(s) *7-10 and 14-92* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5,6 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2007* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7-28-04,8-3-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I (claims 1-6 and 11-13) in the reply filed on 5-9-07 is acknowledged.

Claims 7-10 and 14-92 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Groups II-VII, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 5-9-07.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirsch (4,704,547 from IDS of 7-28-04) in view of Davis (5,455,732).

Kirsch teaches a protection circuit associated with transistors of a voltage specification of a first level, with the protection circuit and the protected transistors being

comprised in an integrated circuit designed to process information. The invention is said to reduce the voltage across one or more transistors in various complementary logic circuits of the type which use NMOS and PMOS transistors. The reduction in voltage across the transistors is achieved while still obtaining a full logic swing at the output of the logic. At col.6, lines 17-35 it is recited that while the description has taught the protection of NMOS devices, the protection of PMOS devices can be similarly provided for by the present technique. A PMOS protective transistor can be provided, serially connected with one or more PMOS logic transistors and having a gate voltage at a desired protective value. The voltages across the transistors described in the teachings are understood to be the "cross terminal voltages" recited in the Applicants claims.

The device taught by Kirsch differs from the claims by not being said to switch off a PMOS device to implement the protective function.

Davis teaches an integrated circuit PMOS and NMOS logic device that protects the transistors against excess cross terminal type voltages by using series connected PMOS transistors that are said to be switched off in response to out of range voltages across the transistor terminals (see col. 5, lines15-20). The Davis teachings are concerned with logic operation in a mixed voltage environment such as a system with 3.3V elements and 5V elements (see abstract).

It would have been obvious to combine the teachings of Davis into the device taught by Kisch because both teachings relate to voltage considerations and protection in logic circuits using NMOS and PMOS transistors, with Davis teaching the switch-off of

a PMOS protection transistor as a way to implement a protective function in an integrated circuit.

With regard to the PMOS transistor limitation of claim 2, both teachings are said to use a PMOS protective device in combination with a PMOS logic element.

With regard to the connection of a PMOS transistor to a supply voltage of a level above the specification of the transistor (claim 3), the operation of the teachings of Davis in the mixed voltage system is seen to address the limitation by the connection of transistors to VCC.

Claim 4 only recites the normal swing of a data signal between zero and a fixed voltage understood to represent a binary "one".

Allowable Subject Matter

Claims 5,6 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 5 adds limitations that would produce an integrated circuit having a mixture of NMOS and PMOS protection transistors in combination with additional protective and logic transistors, which is described in a manner that is not seen to be conventional practice in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Jackson whose telephone number is 571-272-2051. The examiner can normally be reached on 6:30am-3:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SWJackson

November 7, 2007

Stephen W Jackson
11-7-07

STEPHEN W. JACKSON
PRIMARY EXAMINER